respectfully disagrees. Claim 1 (and similarly Claim 12) recites: a "signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits." Evoy is silent concerning timing of arbitration logic 203. The Examiner cites Evoy col. 4, lines 1-20 as supporting the rejection and claims that the above-recited limitations are "inherent". Applicant respectfully point out that while Evoy states that arbitration logic 203 avoids conflicts between the devices in relation to the shared pins (Evoy col. 4, lines 11-12), Evoy does not teach that early enabling and late disabling consistent with the setup and hold times of the devices is performed, only that conflicts between the devices are prevented, indicating the arbitration logic 203 only permits one "owner" of a pin at a time. Neither are such features inherent in the device of Evoy, as the presence of arbitration between devices does not necessarily imply that the early enabling and late disabling of the present invention are present in arbitration logic 203. To support a rejection under 35 U.S.C. 102(b), the reference must show each and every element of the claim rejected. The Examiner has not met this burden, as the argument that the signal means features of the present invention are inherent in arbitration logic 203 of Evoy cannot be shown within the confines of Evoy as Evoy does not disclose details of a structure in which such features are inherent, as arbitration logic 203 could be designed

without the above-described limitations.

Therefore, Applicant believes that the rejection under 35 U.S.C. §102(b) is unsupported by Evoy and therefor has been overcome.

3. Rejections under 35 U.S.C. §103

Under 35 U.S.C. §103(a), The Examiner has rejected Claim 3 as being unpatentable over Evoy in view of Chan, et al. (US 2002/0052990), Claim 5 as being unpatentable over Evoy in view of Clark, et al. (US 2001/0005225), Claim 6 as being unpatentable over Evoy in view of Hough (US 6,324,596), Claim 8 as being unpatentable over Evoy in view of Clark in further view of Richard (4,756,006), Claim 9 Claim as being unpatentable over Evoy in view of Gradinariu (US 6,378,008), Claim 10 as being unpatentable over Evoy in view of Gradinariu in further view of Richard and Claim 11 as being unpatentable over Evoy in view of Clark in further view of in further view of Kudou (US 5,363,494). Applicant respectfully disagrees with all of the above rejections.

None of the above-cited references teach the "signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits" recited in the independent claims, and none of them teach interface pin sharing in the context of the present invention at

all. Chan, Houg and Richard teach bus interface connections, but not a bus interface sharing a pin between two internally multiplexed signals targeting different peripherals and neither does Clark, Grandinaru or Kudou. Clark teaches a system of CMOS image sensors, not computer bus pin-sharing at all nor is the technology so related that there would be any motivation to combine Clark with Evoy.

Further, Kudou, cited by the Examiner as providing the transmission gate for interfacing a bidirectional signal of Claim 11. Applicant respectfully points out that in Kudou, the bi-directional buffer is enabled for one direction of data flow at a time, and therefore would does not provide the functionality of a transmission gate as in the present invention, wherein signal flow is enabled in both directions simultaneously with respect to the interface pin. Similarly, while Grandinaru teaches a pair of tri-state buffers, the output buffer is coupled to another bus line, not the same bus line as in the present invention. Therefore neither Kudou nor Grandinaru provide further support for the rejection of Claims 9-11 and Applicant believes that for that reason, as well as the arguments stated above with respect to the signal means recited in Claim 1, that Claims 9-11 should be allowed.

Applicant respectfully points out that in addition to showing the existence of an element in a secondary or tertiary reference, the Examiner must show that there exists a motivation

to combine the teachings of the reference, absent hindsight of the particular combination of the elements as revealed by the Claims. None of the above references show a motivation to combine any of their teachings with the teachings of Evoy and further, Evoy does not mention such motivation, particularly with respect to the sharing of an interface pin with respect to a bi-directional signal as recited in Claim 11, as Evoy is silent as to sharing interface pins carrying a fully bi-directional signal to and from one or more of the devices. Also, with respect to the rejection of Claim 8, none of the references Evoy, Clark or Richard demonstrate a motivation to include a latch for each signal input to the interface so that a state of two shared input signals can be maintained within the interface.

Therefore, for all of the reasons stated above, Applicant believes that the rejections under 35 U.S.C. §103 have been overcome.

Similarly, new Claims 13-20 all recite features as indicated for Claims 1 and 12 above and should therefore be found allowable.

CONCLUSION

In conclusion, Applicant respectfully submits that this Amendment, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicant respectfully submits that he has demonstrated that the above-identified Patent Application, including Claims 1-20 is in condition for allowance. Such action is earnestly solicited.

No fee is believed to be required in connection with this Amendment, as the total number of claims does not exceed 20 and the number of independent claims does not exceed 3. However, if there are any fees incurred by this Amendment Letter, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,

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